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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,931	03/19/2004	Masaaki Yoshida	R2184.0307/P307	6728

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EXAMINER	
MENZ, DOUGLAS M	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,931	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Douglas M. Menz	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *9-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-6 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (APA).

Regarding claim 1, APA discloses a semiconductor device comprising:

A substrate (10, Prior Art Fig. 1); and

At least three kinds of wells (12, 20, 5c, Prior Art Fig. 1) formed in and on a top surface of the substrate (10, Prior Art Fig. 1),

Wherein at least one kind of well (12, Prior Art Fig. 1) has a top surface height level higher than the top surface height levels of the other two kinds of wells (20, 5c, Prior Art Fig. 1) in relation to the top surface of the substrate, wherein the other two kinds of wells have a different conductivity type (NW) than the at least one kind of well (PW, Prior Art Fig. 1).

Regarding claim 2, APA further discloses wherein said other two kinds of wells (20, 5c, Prior Art Fig. 1) have the same conductivity type (NW) and have different impurity concentrations with relation to each other (Prior Art Fig. 1).

Regarding claim 3, APA further discloses wherein at least one kind of well (5c,Prior Art Fig. 1) has an impurity concentration that is decreased to a level necessary to form a high-voltage transistor (Prior Art Fig. 1 and page 3 of the specification).

Regarding claim 4, APA further discloses wherein said other two kinds of wells (20, 5c, Prior Art Fig. 1) have different junction depths within the substrate relative to each other.

Regarding claim 5, APA further discloses wherein one of said other two kinds of wells (5c, Prior Art Fig. 1) has a larger junction depth within the substrate and further includes a triple well in which a well of an opposite conductivity type (12, Prior Art Fig. 1) having a smaller junction depth is formed.

Regarding claim 6, APA further discloses wherein said at least one kind of well (12, Prior Art Fig. 1) and said other two kinds of wells (20, 5c, Prior Art Fig. 1) are of different conductivity types to each other (P-well, N-well, respectively, Prior Art Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Hirase (US 6107672).

Regarding claim 7, APA discloses the structure of claim 1 as mentioned above, APA further discloses that the triple well structures are widely used in digital/analog mixed LSI and memory mixed LSI (APA Specification page 3), however, APA does not explicitly disclose wherein a MOS transistor is formed by a drain diffusion layer and a source diffusion layer formed in the more than three kinds of wells and a gate electrode formed on areas corresponding to the drain diffusion layer and the source diffusion layer via a gate insulating film. These MOS transistor features are well known in the art and

as an example, Hirase discloses an at least three well structure wherein a MOS transistor is formed by a drain diffusion layer and a source diffusion layer formed in the more than three kinds of wells (3,4,5,6 and 7) and a gate electrode formed on areas corresponding to the drain diffusion layer and the source diffusion layer via a gate insulating film (Figs.1, 4 and Cols. 5-6 and Cols. 9-10).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the specifics of Hirase's structure into the multiple well structure of APA as this is expressly suggested by APA (specification page 3).

Regarding claim 8, APA discloses the structure of claim 5 as mentioned above, APA further discloses that the triple well structures are widely used in digital/analog mixed LSI and memory mixed LSI and mixing power supply circuits and is capable of shielding noise (APA Specification page 3), however, APA does not explicitly disclose wherein MOS transistors are formed by drain diffusion layers and source diffusion layers formed in the more than three kinds of wells and gate electrodes formed on areas corresponding to the drain diffusion layers and the source diffusion layers via a gate insulating film, and wherein one of the MOS transistors formed on the triple well is one of a MOS transistor constituting a power supply circuit, a MOS transistor constituting a circuit sensitive to a substrate noise and a MOS transistor constituting a circuit generating a noise. Hirase discloses wherein MOS transistors are formed by drain diffusion layers and source diffusion layers formed in the more than three kinds of wells (3,4,5,6 and 7) and gate electrodes formed on areas corresponding to the drain

diffusion layers and the source diffusion layers via a gate insulating film, and wherein one of the MOS transistors formed on the triple well is one of a MOS transistor constituting a power supply circuit, a MOS transistor constituting a circuit sensitive to a substrate noise and a MOS transistor constituting a circuit generating a noise (Figs.1, 4 and Cols. 5-6 and Cols. 9-12).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the specifics of Hirase's structure into the multiple well structure of APA as this is expressly suggested by APA (specification page 3).

Response to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CHRISTIAN D. WILSON
PRIMARY EXAMINER

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